PTO/SB/08A (05-03)

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1.				Application Number	TBD 18/148445		
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	STATEMENT BY APPLICANT			First Named Inventor	u		
				Art Unit	TBD		
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Sheet	1	of	1	Attorney Docket Number	2003 P 54309 US		

			U.S. PATENT	DOCUMENTS	
Examiner	Cite No.1	Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where
Initials*		Number - Kind Code ^{2 (Fknown)}	MM-DD-YYYY	Applicant of Cited Document	Relevant Passages or Relevant Figures Appear
DHIL	1	US-6,621,131 B2	09-18-2003	Murthy, et al.	
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		FOREIG	N PATENT DOCU	IMENTS		
Examiner Initials*	0.3-	Foreign Patent Document	Publication Date	Name of Patentee or	Pages, Columns, Lines,	T
	Cite No.1	Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)	MM-DD-YYYY	Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear	T ⁶
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		OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS	
Examiner Initiats*	Cite, No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
PHK	2	ERNST, T., et al., "A New Si:C Epitaxial Channel nMOSFET Architecture with Improved Drivability and Short-Channel Characteristics," 2003 Symposium on VLSI Technology Digest of Technical Papers, 4-89114-035-6/03.	
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Examiner Signature		Date Considered	04-22-05
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INFORMATION DISCLOSURE				Application Number	10/748,995
				Filing Date	December 30, 2003
	STATEMENT BY APPLICANT			First Named Inventor	LI
				Art Unit	TBD
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Sheet	1	of	1	Attorney Docket Number	2003 P 54309 US

			U.S. PATENT I	DOCUMENTS	
Examiner Initials*	C210	Document Number	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where Relevant Passages or Relevant
	Cite No.1	Number - Kind Code ^{2 (d known)}	MM-OD-YYYY	Applicant of Cited Document	Relevant Passages or Relevant Figures Appear
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Examiner	Cite	item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-tasue	T ²
Initials* No	No.	number(s), publisher, city and/or country where published.	
pn4	1	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2003 Edition, pp. 23–25, http://member.itrs.net/.	
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